KANNUR UNIVERSITY

Faculty of Engineering

Curriculum, Scheme of Examinations and Syllabi for M. Tech. Degree Program with effect from Academic Year 2012-2013

Electronics & Communication Engineering

M. Tech.

in

Signal Processing and Embedded Systems

FIRST SEMESTER

Code	Subject	Hours/Week			Sessional Marks	University Examination		Credit
		L	T	P		Hrs	Marks	
SPE 101	Linear Algebra for Signal Processing	3	-	-	50	3	100	3
SPE 102	Random Processes and Applications	3	-	-	50	3	100	3
SPE 103	Design using Embedded Processers	3	-	-	50	3	100	3
SPE 104	DSP and Applications	3	-	-	50	3	100	3
SPE 105	Elective I	3	-	-	50	3	100	3
SPE 106	Elective II	3	-	-	50	3	100	3
SPE 107 (P)	Digital Signal Processing Lab	-	-	2	50	3	100	2
SPE 108 (P)	Seminar	-	-	2	50	-	-	2
TOTAL		**18**		**4**	**400**		**700**	**22**

ELECTIVE-I

SPE 105 (A) Digital VLSI Design

SPE 105 (B) DSP Processors and Architecture

SPE 105 (C) High Speed Digital Design

SPE 105 (D) Multi-rate Signal Processing

ELECTIVE II

SPE 106 (A) Biomedical Signal Processing and Systems

SPE 106 (B) Advanced Digital System Design

SPE 106 (C) Adaptive Signal Processing

SPE 106 (D) Analog Integrated Circuit Design

SECOND SEMESTER

Code	Subject	Hours/Week			Sessional Marks	University Examination		Credit
		L	T	P		Hrs	Marks	
SPE 201	Digital Image Processing	3	-	-	50	3	100	3
SPE 202	Wavelet Theory	3	-	-	50	3	100	3
SPE 203	Embedded Systems	3	-	-	50	3	100	3
SPE 204	Elective III	3	-	-	50	3	100	3
SPE 205	Elective IV	3	-	-	50	3	100	3
SPE206	Elective V	3	-	-	50	3	100	3
SPE 207 (P)	VLSI & Embedded Systems Lab	-	-	2	50	3	100	2
SPE 208 (P)	Term Paper	-	-	2	50	-	-	2
TOTAL		**18**		**4**	**400**		**700**	**22**

ELECTIVE-III

SPE 204 (A) Statistical Signal Processing

SPE 204 (B) CMOS Mixed Signal Circuit Design

SPE 204 (C) Multimedia Systems

SPE 204 (D) ASIC Design

ELECTIVE-IV

SPE 205 (A) Speech Processing

SPE 205 (B) Low Power VLSI Design

SPE 205 (C) Biometric Processing

SPE 205 (D) Introduction to Nano Electronics

ELECTIVE-V

SPE 206 (A) Pattern Recognition and Computer Vision

SPE 206 (B) Research Methodologies

SPE 206 (C) Embedded Networks

SPE 206 (D) VLSI System Design

THIRD SEMESTER

Code	Subject	Hrs / Week			Marks					Credits
		L	T	P	Internal		University		Total	
					Guide	Evaluation Committee	Thesis	Viva		
SPE 301 (P)	Thesis Preliminary			22	200	200	--	--	400	8
	Total			**22**	**200**	**200**			**400**	**8**

THESIS PRELIMINARY

This shall comprise of two seminars and submission of an interim thesis report. This report shall be evaluated by the evaluation committee. The fourth semester Thesis- Final shall be an extension of this work in the same area. The first seminar would highlight the topic, objectives, methodology and expected results. The first seminar shall be conducted in the first half of this semester. The second seminar is presentation of the interim thesis report of the work completed and scope of the work which is to be accomplished in the fourth semester.

FOURTH SEMESTER

Code	Subject	Hrs / Week			Marks					Credits
		L	T	P	Internal		University		Total	
					Guide	Evaluation Committee	Thesis	Viva		
SPE 401 (P)	Thesis			22	200	200	100	100	600	12
	Total			**22**	**200**	**200**	**100**	**100**	**600**	**12**

THESIS

Towards the middle of the semester there shall be a pre submission seminar to assess the quality and quantum of the work by the evaluation committee. This shall consist of a brief presentation of Third semester interim thesis report and the work done during the fourth semester. The comments of the examiners should be incorporated in the work and at least one technical paper is to be prepared for possible publication in journals / conferences. The final evaluation of the thesis shall be an external evaluation.

Sessional marks for all the Theory based Subjects

The marks allotted for internal continuous assessment and end-semester university examinations shall be 50 marks and 100 marks respectively with a maximum of 150 marks for each theory subject.

The weightage to award internal assessment marks should be as follows:

Test papers (two tests) : 25 marks

Assignments and/or class performance : 25 marks

Sessional marks for all the Practical Subjects

The marks allotted for internal continuous assessment and end-semester university examinations shall be 50 marks and 100 marks respectively with a maximum of 150 marks for each practical subject.

The weightage to award internal assessment marks should be as follows:

Test paper : 15 marks

Laboratory class work and records : 35 marks

SPE 101/CSP 101 LINEAR ALGEBRA FOR SIGNAL PROCESSING

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in Matrix Theory at UG level

Objective: To have an advanced level knowledge on linear algebra and its applications in signal processing.

Algebraic Structures: - Sets, Functions, Cardinality of sets, Groups, Rings, Fields, Vector spaces, Subspaces, Basis and dimension, Finite and infinite dimensional vector spaces.

Linear transformations: Linear Transformations, Sum, product and inverse of Linear Transformations, Rank-nullity theorem, Isomorphism, Matrix representation of Linear Transformations, Four fundamental subspaces of Linear Transformations, Change of bases, Linear functional.

Metric space and Hilbert space : Metric space, Open sets, Closed sets, Neighborhoods, Sequences , Convergence, Completeness, Continuous mappings, Normed space, Banach space, L^p space and l^p space, Inner product space, Hilbert space, Signal space, Properties of inner product space, Orthogonal compliments and direct sums, Orthonormal sets, Gramm-Schmidt orthonormalization process, Projections.

Matrix Theory –Matrix rank, Solving linear system of equations using matrices, LDU factorisation, QR decomposition, Least square approach, Eigen values, Eigen vectors and spectrum, Diagonalizability, Orthogonal diagonalization, Properties of Eigen values and Eigen vectors of Hermitian matrices, Normal matrices, Unitary matrices, Multiresolution analysis and wavelets.

References:

1. Hoffman Kenneth and Kunze Ray, *Linear Algebra,* Prentice Hall of India.
2. Erwin Kreyzig, *Introductory Functional Analysis with Applications*, John Wiley, 2006.
3. G.F.Simmons, *Topology and Modern Analysis* , McGraw Hill.
4. Frazier, Michael W. *An Introduction to Wavelets through Linear Algebra,* Springer Publications.
5. Strang G, *Linear Algebra and its Applications*, 3rd edition, Saunders, 1988.
6. Jin Ho Kwak&Sungpyo Hong, *Linear Algebra*, Springer International, 2004.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 102/CSP 102 RANDOM PROCESSES AND APPLICATIONS

3 hours lecture per week	L-3	T-0	P-0	C-3

Prerequisite: Basic knowledge in Set theory and Probability at UG level

Objective: To impose in depth knowledge of random process and its applications.

Review of set theory, probability and random variables: Review of Set Theory: Set operations, functions, countable and uncountable sets, Random experiment, Sample space, Sigma algebra, Event space, Measure, Probability measure, Borel sigma field, Probability Distribution Function, CDF, PDF and PMF, Joint cdf, joint pdf, conditional distribution and expectation. Expectation: Fundamental Theorem of expectation, moments, characteristic function, correlation and covariance

Random Vector: - Definition, Joint statistics, Covariance and correlation matrix, Gaussian random vectors.

Convergence: - Markov and Chebyshev inequalities, Convergence of sequences of random variables- almost sure convergence, convergence in probability, convergence in mean square, Weak law of large numbers, Random sums, Borel Cantelli lemma, strong law of large numbers, Central Limit Theorem for sequences of independent random variables.

Random process:- Definition of Random process, IID process, Poisson counting process, Markov process, birth-death process, Wiener process. Stationarity, Correlation functions of random processes in linear systems, power spectral density.

Discrete Time Markov Chains: conditional independence, DTMC, Recurrence analysis, Foster's Theorem, Chapman-Kolmogov theorem, Stopping time, classification of states: absorbing, recurrent, transient. Communicating classes, Continuous time Markov chains, Poisson process, simple Markovian queues.

References :

1. B. Hajek, *An Exploration of Random Processes for Engineers*, 2005.
2. D.P. Bertsekas and J. N. Tsitsiklis, *Introduction to Probability*, 2000.
3. Gray, R. M. and Davisson L. D., *An Introduction to Statistical Signal Processing.* Cambridge University Press, 2004.
4. Stark Henry, *Probability and Random Processes With Application to Signal Processing,* 3/e, Pearson Education India.
5. Steven Kay, *Intuitive probability and random processes using Matlab*, Springer, 2006.

Reading :

1. Dr. Kishor S. Trivedi. *Probability and Statistics with Reliability, Queuing, and Computer Science Applications,* John Wiley and Sons, New York, 2001.
2. Athanasios Papoulis and S. UnnikrishnaPillai. *Probability, Random Variables and Stochastic Processes,* TMH.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 103 DESIGN USING EMBEDDED PROCESSERS

3 hours lecture per week	L-3	T-0	P-0	C-3

Prerequisite: Basic Knowledge in Digital electronics and Microprocessors at UG level

Objective: To develop skills in designing complex systems using different processor architectures.

Introduction to Embedded system: Embedded system examples, Parts of Embedded System Typical Processor architecture, Power supply, clock, memory interface, interrupt, I/O ports, Buffers, Programmable Devices, ASIC, etc. Simple interfacing examples. Memory Technologies – EPROM, Flash, OTP, SRAM, DRAM, SDRAM etc.

Introduction to PIC microcontrollers: CPU architecture, registers, memory, instruction sets , addressing modes, timers, Interrupts, I/O, I 2C Bus Operation, Serial EEPROM,PWM, Analog to digital converter, UART,SPI.

ARM architecture: ARM organization and Implementation, Memory Hierarchy, ARM Instruction Set and Thumb Instruction set, Assembly Language Programming, High- Level Language Programming, System Development using ARM. Digital Signal Processing on ARM. Peripheral Programming and system design for a specific ARM processor (ARM7/9).

Embedded System product Development: Embedded System product Development Life cycle (EDLC), Specifications, Component selection, Schematic Design, PCB layout, fabrication and assembly. Product enclosure design and development. Concept of firmware, operating system and application programs. Power supply Design. External Interfaces.

Embedded System Development Environment – IDE, Cross compilation, Simulators/Emulators, Hardware Debugging. Hardware testing methods like Boundary Scan, In Circuit Testing (ICT) etc.

Bus architecture like I^2C, SPI, AMBA, CAN etc.

References:

1. Shibu K.V. Introduction to Embedded Systems Tata McGraw Hill, 2009.
2. Tim Wilmshurst, An introduction to the design of small-scale embedded systems Palgrave.
3. Design with PIC microcontrollers John B Peatman Pearson Education Asia 2002.
4. Van Ess, Currie and Doboli Laboratory Manual for Introduction to Mixed-Signal, Embedded Design, Alphagraphics, USA.
5. Steve FurberARM System-on-chip Architecture **,**Second Edition Pearson Education,2007.
6. William HohlARM Assembly Language Programming CRC Press,2009.
7. Andrew Sloss, DominicSymes, Christ Wright ARM System Developer's guide –Designing and optimizing software Elseiver Publishers ,2008.
8. Web Based Resources.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 104 DSP AND APPLICATIONS

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in signals and systems at UG level

Objective: To attain a good analytical ability in digital filter design

Review of Transform Theory: Continuous Time Signals-Laplace Transform- Fourier Transform-Sampling Theory-Discrete Time Signals-Z-Transform-ROC-Poles & Zeros-Discrete Time Fourier Transform-DFT-Efficient Computation-FFT-Discrete Cosine Transform-Short Time Fourier Transform.

Design of FIR filters: Specifications. Coefficient calculation methods-Windowing, Optimal and Frequency sampling methods- Comparison of different methods- Realization structures-Finite word length effects-Implementation techniques-Examples. FIR filter design with Matlab. Implementation of FIR filter in general purpose digital signal processors.

Design of IIR filter: Specifications. Coefficient calculation methods-Pole zero placement, Impulse invariant, Matched Z transform and Bilinear Z transform(BZT)-Design using BZT and classical analog filters-IIR filter coefficients by mapping S plane-Poles and Zeros-Realization structures-Finite word length effects-Implementation techniques-Examples-IIR filter design with Matlab. Implementation of IIR filter in general purpose digital signal processors.

Adaptive Digital Filters: Concepts -Wiener filter-LMS adaptive algorithm-Recursive least squares algorithm-Lattice Ladder filters-Application of Adaptive filters.

Power Spectrum Estimation: Estimation of spectra from finite-duration signals- Non-parametric and Parametric methods for Power Spectrum Estimation.

References:

1. Emmanuel C. Ifeachor and Barrie W. Jervis, *Digital Signal Processing, A practical Approach*, 2/e, Pearson Education.

2. J. G. Proakis and D. G. Manolakis, *Digital Signal Processing: Principles, Algorithms, and Applications*, 4/e, Pearson Education.

3. Johnny R. Johnson, *Introduction to Digital Signal Processing*, PHI, 1992.

4. Ashok Ambardar, *Digital Signal Processing: A Modern Introduction*, Thomson, IE, 2007.

Reading:

1. Douglas F. Elliott, *Handbook of Digital Signal Processing- Engineering Application*, Academic Press.

2. Robert J. Schilling, Sandra L. Harris, *Fundamentals of Digital Signal Processing using MATLAB*, Thomson, 2005.

3. Ingle, J. G. Proakis, *Digital Signal Processing Using MATLAB*, Thomson, 1/e.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 105 (A) DIGITAL VLSI DESIGN

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in Solid State Devices and Digital Electronics at UG level

Objective: To impart skills in developing digital integrated circuits.

Introduction MOSFET: threshold voltage, current, Channel length modulation, body bias effect and short channel effects, MOS switch, MOSFET capacitances, MOSFET models for calculation-Transistors and Layout, CMOS layout elements, parasitics, wires and vias-design rules-layout design SPICE simulation of MOSFET I-V characteristics and parameter extraction

CMOS inverter: static characteristics, noise margin, effect of process variation, supply scaling, dynamic characteristics, inverter design for a given VTC and speed, effect of input rise time and fall time, static and dynamic power dissipation, energy & power delay product, sizing chain of inverters, latch up effect-Simulation of static and dynamic characteristics, layout, post layout simulation

CMOS design: Static CMOS design, Complementary CMOS, static properties, propagation delay, Elmore delay model, power consumption, low power design techniques, logical effort for transistor sizing, ratioed logic, pseudo NMOS inverter, DCVSL, PTL, DPTL & Transmission gate logic, dynamic CMOS design, speed and power considerations, Domino logic and its derivatives, C2MOS, TSPC registers, NORA CMOS – Course project

Circuit design considerations: Arithmetic circuits, shifter, CMOS memory design - SRAM and DRAM, BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic

References:

1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, MGH, Third Ed., 2003.

2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Prentice Hall, Second Edition, 2005.

3. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital Integrated Circuits, Third Edition, McGraw-Hill, 2004.

4. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation, Wiley-IEEE Press, 2007.

5. Christopher Saint and Judy Saint, IC layout basics: A practical guide, McGraw-Hill Professional, 2001.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 105 (B)/CSP 104 DSP PROCESSORS AND ARCHITECTURE

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in DSP and microprocessors at UG level

Objective: To have an in depth knowledge in DSP at processor level

Review of Pipelined RISC Architecture and Instruction Set Design.

Performance and Benchmarks - SPEC CPU 2000, EEMBC DSP benchmarks.

Basic Pipeline: Implementation Details - Pipeline Hazards (based on MIPS 4000 arch).

Instruction Level Parallelism (ILP) - Concepts, Dynamic Scheduling – Tomasulo's algorithm-Reducing Data hazards. Dynamic Hardware Prediction - Reducing Branch Hazards. Multiple Issue-Hardware-based speculation. Limitations of ILP.

Review of Memory Hierarchy - Cache design, Cache Performance Issues & Improving Techniques.

Computer arithmetic- Signed Digit Numbers(SD) - Multiplier Adder Graph - Logarithmic and Residue Number System(LNS, RNS) - Index Multiplier –Architecture for Pipelined Adder, Modulo Adder & Distributed Arithmetic(DA), CORDIC Algorithm and architecture

Case studies - Introduction to TMS 320 C 6X Processor – Architecture – Functional units - pipelining –Registers –Linear and Circular addressing modes –Types of instructions –sample program, Overview of BlackFin processor

References :

1. J. L. Hennesy and D. A. Patterson, *Computer Architecture A Quantitative Approach,* 3/e, Elsivier India, Chapter 1, Appendix A, Chapter 3, Chapter 5.
2. U. Mayer-Baese, Digital Signal Processing with FPGAs, Springer, 2001.
3. RulphChassaing, Digital signal Processing and Applications with the C6713 and C6416 DSK – Wiley Interscience.

Reading :

1. *Blackfin Processor Hardware Reference, Analog Devices, Version 3.0*, 2004 (Section 2.3-2.53, 4.7-4.15, 6.1 -6.53).
2. D. VenkatRemani and M. Bhaskar, *Digital Signal Processor: Architecture Programming and Applications*, Tata McGrawHill, 2002.
3. Phil Lapsley, J. Bier, AmitSohan and Edward A. Lee, *DSP Processor fundamentals : Architecture and Features.* Wiley IEEE Press.
4. Sen M. Kuo, Woon-seng S. Gan, *Digital Signal Processors*, Prentice Hall.
5. Processor Manuals.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 105 (C) HIGH SPEED DIGITAL DESIGN

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in Digital Electronics and Network Theory at UG level

Objective: To attain good analytical skills in digital integrated circuit and PCB design

Introduction to high-speed digital design: Frequency, time and distance - Capacitance and inductance effects - High seed properties of logic gates - Speed and power -Modelling of wires - Geometry and electrical properties of wires - Electrical models of wires - transmission lines - lossless LC transmission lines - lossy LRC transmission lines - special transmission lines

Power distribution and noise: Power supply network - local power regulation - IR drops - area bonding - onchip bypass capacitors - symbiotic bypass capacitors - power supply isolation - Noise sources in digital system - power supply noise - cross talk – inter symbol interference

Signalling convention and circuits: Signalling modes for transmission lines -signalling over lumped transmission media - signalling over RC interconnect - driving lossy LC lines - simultaneous bi-directional signalling - terminations - transmitter and receiver circuits

Timing convention and synchronisation: Timing fundamentals - timing properties of clocked storage elements - signals and events -open loop timing level sensitive clocking - pipeline timing - closed loop timing - clock distribution - syncronisation failure and metastability - PLL and DLL based clock aligners

References:

1. William S. Dally & John W. Poulton, Digital Systems Engineering, Cambridge University Press, 1998.
2. Howard Johnson & Martin Graham; High Speed Digital Design: A Handbook of Black Magic, Prentice Hall PTR, 1993.
3. Masakazu Shoji; High Speed Digital Circuits, Addison Wesley Publishing Company, 1996.
4. Jan M, Rabaey, et all; Digital Integrated Circuits: A Design perspective, Second Edition, 2003.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 105 (D) MULTI-RATE SIGNAL PROCESSING

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in DSP at UG level

Objective: To attain in depth knowledge in digital filter banks

Fundamentals of Multi-rate Theory: The sampling theorem - sampling at sub Nyquist rate - Basic Formulations and schemes.

Basic Multi-rate operations- Decimation and Interpolation - Digital Filter Banks- DFT Filter Bank- Identities- Poly phase representation.

Maximally decimated filter banks: Poly phase representation - Errors in the QMF bank- Perfect reconstruction (PR) QMF Bank - Design of an alias free QMF Bank.

M-channel perfect reconstruction filter banks

Uniform band and non uniform filter bank - tree structured filter bank- Errors created by filter bank system- Poly phase representation- perfect reconstruction systems.

Perfect reconstruction (PR) filter banks

Para unitary PR Filter Banks- Filter Bank Properties induced by para unitarity- Two channel FIR para unitary QMF Bank- Linear phase PR Filter banks- Necessary conditions for Linear phase property- Quantization Effects: -Types of quantization effects in filter banks. Coefficient sensitivity effects, dynamic range and scaling.

Cosine Modulated filter banks

Cosine Modulated pseudo QMF Bank- Alas cancellation- phase - Phase distortion- Closed form expression- Poly phase structure- PR Systems

References:

1. P.P. Vaidyanathan, “Multirate systems and filter banks.” Prentice Hall. PTR. 1993.

2. N.J. Fliege, “Multirate digital signal processing .” John Wiley 1994.

3. Sanjit K. Mitra, “ Digital Signal Processing: A computer based approach.” McGraw Hill. 1998.

4. R.E. Crochiere. L. R. “Multirate Digital Signal Processing”, Prentice Hall. Inc.1983.

5. J.G. Proakis. D.G. Manolakis, “Digital Signal Processing: Principles. Algorithms and Applications”, 3rd Edn. Prentice Hall India, 1999.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 106 (A)/CSP 106 (C) BIOMEDICAL SIGNAL PROCESSING AND SYSTEMS

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge of bio-signals and random signals at UG level.

Objective: To attain good analytical knowledge in modeling bio-medical systems.

Introduction to bio signals- generation of bio signals-action potential, resting membrane potential, ECG-data acquisition, lead system, arrhythmias; EEG signals and characteristics, evoked potential.

Computerized data acquisition system - basic requirements, Preprocessing of biosignals- removal of interferences due to power line & Electro Surgical Unit, Adaptive filtering- fetal heart rate monitoring -a case study

Statistical Signal Processing - Introduction to random signals and its characteristics, properties of random signals, moments of signal, Concepts of PDF, autocorrelation, cross correlation, covariance, estimation of power spectral density-parametric& non-parametric, Wiener filter, implementation of algorithm for autocorrelation and PSD using MATLAB.

Analysis of bio signals – ECG- continuous monitoring, arrhythmia detection- algorithms and methods, HRV signal. EEG- video EEG, analysis of epilepsy using EEG.

Prediction- Modeling of bio signals –linear models- AR model, MA model and ARMA model, Modeling of ECG signal using MATLAB

Non stationary signal analysis: Time domain methods, frequency domain methods, time-frequency methods, wavelets

Classification - introduction to ANN and Fuzzy logic, algorithm for Arrhythmia classification

Introduction to nonlinear analysis of bio signals - chaos, Analysis of heart rate variability and blood pressure variability using measures based on chaotic theory.

References:

1. Willis J. Tompkins**,** *Biomedical Digital Signal Processing* , Prentice Hall of India publications/ Eastern Economy Edition, 2nd Print, 2000.
2. Petre Stoica and Randolph Moses , Spectral Analysis of Signals, Prentice Hall, 2005.
3. D. C. Reddy, *Biomedical Signal Processing Principles and Techniques* , TMH, 2005.
4. Rangaraj M. Rangayyan ,*Biomedical Signal Analysis - A case study approach* , John Wiley, 2002.
5. A. Cohen, *Biomedical Signal Processing* Vol. I & II, CRC Press, 2002.
6. M. Akay, *Detection and estimation of biomedical signals*, Academic Press, 1996
7. John L Semmlow, *Biosignal and Biomedical Image Processing: MATLAB-Based Applications*, Dekker/CRC Press, 2004.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 106 (B) ADVANCED DIGITAL SYSTEM DESIGN

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in Digital System Design at UG level

Objective: To attain knowledge in designing and testing programmable logic devices.

Hardware Description Languages: Introduction to VHDL/VERILOG - Behavioral Modeling - Transport vs Inertial Delay - Simulation Deltas - Sequential Processing - Process Statement - Signal Assignment vs Variable Assignment - Sequential Statements - Data Types - Assert and report statements Subprograms and Packages - Predefined Attributes - Configurations - Subprogram Overloading - VHDL synthesis - Design Examples-–new developments in HDLs

Finite State machines: Design of FSMs–state tables –state graphs – General models for sequential networks - Derivations of State Graphs and Tables. Reduction of state Tables State Assignment - Sequential Network Design. Design examples using the FSM approach –sequence detector, serial adders, multipliers, dividers. Design using ASM charts –realization of SM charts –example designs

Impediments to Synchronous design: Clock Skew, Gating the clock, Asynchronous inputs, Synchronizer Failure and Metastability: Synchronizer failure, Metastability Resolution Time, Reliable Synchronizer Design, Analysis of Metastable timing , Better synchronizers, Metastable hardened flip flops , Synchronizing High Speed data transfers. Timing hazards : Static Hazards, Finding static hazards, Dynamic Hazards, Designing hazard free circuit

Designing With Programmable Devices: Programmable LSI Techniques - Programmable Logic Arrays - Programmable Array Logic - Sequential PLDs - Sequential Circuit Design using PLDs - Complex Programmable Logic Devices and FPGAs- Altera Series FPGAs and Xilinx Series FPGAs

Design Issues For Testability : Introduction to Testing and Diagnosis Fault modeling : Logical fault models - Fault Detection and Redundancy - Fault Equivalence and Fault Location - Fault Dominance - Single stuck model - Multiple stuck model - Bridging faults Design for Testability: Testability -Ad hoc Design - Scan Registers and scan techniques -Boundary scan standards Built in Self Test: Introduction - Test Pattern generation -Generic Off line BIST Architectures Compression Techniques -General aspects -Signature Analysis

References:

1. J. Bhasker; A VHDL Primer, Pearson Education, 2000
2. John F Wakerley ,Digital Design Principles and Practice –4th Edition , Pearson education ,2006
3. Charles H Roth ,Jr , Digital Design using VHDL , Cenage Publishers ,India Edition,2006
4. Kenneth L Short , VHDL for Engineers , Pearson Education ,2009
5. Mark Zwolinski ,Digital System Design with VHDL –Pearson Education,2004
6. MironAbramovici, Melvin Breuer, Arthur D Friedman ,Digital Systems Testing and Testable Design –Jaico Publishing House,2005

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 106 (C) ADAPTIVE SIGNAL PROCESSING

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in DSP and linear algebra at UG level.

Objective: To build a good foundation in adaptive signal processing.

Adaptive systems - definitions and characteristics - applications - properties-examples - adaptive linear combiner-input signal and weight vectors - performance function-gradient and minimum mean square error -introduction to filtering-smoothing and prediction - linear optimum filtering-orthogonality - Wiener – Hopf equation-performance surface

Searching performance surface - stability and rate of convergence - learning curve-gradient search - Newton's method - method of steepest descent - comparison - gradient estimation - performance penalty - variance -excess MSE and time constants – mis-adjustments

LMS algorithm - convergence of weight vector-LMS/Newton algorithm - properties - sequential regression algorithm - adaptive recursive filters - random-search algorithms - lattice structure – Kalman filters-recursive minimum mean square estimation for scalar random variables- statement of Kalman filtering problem-innovation process-estimation of the state-filtering-initial conditions-Kalman filter as the unifying basis for RLS filters

Applications - adaptive modeling and system identification-adaptive modeling for multipath communication channel, geophysical exploration, FIR digital filter synthesis, inverse adaptive modeling, equalization, and deconvolution-adaptive equalization of telephone channels-adapting poles and zeros for IIR digital filter synthesis

References:

1.Bernard Widrow and Samuel D. Stearns, “Adaptive Signal Processing”, Person Education, 2005.
2.Simon Haykin, “ Adaptive Filter Theory”, Pearson Education, 2003.
3.John R. Treichler, C. Richard Johnson, Michael G. Larimore, “Theory and Design of Adaptive Filters”,Prentice-Hall of India, 2002
4.S. Thomas Alexander, “ Adaptive Signal Processing - Theory and Application”, Springer-Verlag.
5.D. G. Manolokis, V. K. Ingle and S. M. Kogar, “Statistical and Adaptive Signal Processing”, McGraw Hill International Edition, 2000.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 106 (D) ANALOG INTEGRATED CIRCUIT DESIGN

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in Solid State Devices and Linear Integrated Circuits at UG level.

Objective: To attain good analytical skills in analog integrated circuit design.

Introduction MOSFET: Threshold voltage, current, Channel length modulation, body bias effect-MOSFET models in saturation, linear and cutoff regions-current sources and sinks - current mirrors - cascode, Wilson current mirrors - voltage references - Supply independent and temperature independent references - Band gap references.

MOS amplifiers: Common source with resistive, diode connected, current source and triode loads, CS with source degeneration, common gate and source follower stages- cascade and folded cascade structures- frequency response of CS, CD and CG configurations – noise in single stage amplifiers.

MOS differential amplifiers: Common mode response – differential pair with MOS loads – Noise in differential pair-CMOS operational amplifiers - One-stage op-amps and two stage op-amps –gain boosting – Miller, Nulling resistor compensation.

CMOS oscillators - ring oscillators - LC oscillators – Colpitts and one-port oscillators – voltage controlled oscillators – tuning in oscillators.

References:

1. David A Johns & Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 2001.
2. Behzad Razavi, Design of Analog CMOS Integrated Circuit, Tata-McGrawHill, 2002.
3. Philip Allen & Douglas Holberg, CMOS Analog Circuit Design, Oxford University Press, 2002.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 107 (P) DIGITAL SIGNAL PROCESSING LAB

2hours practical per week	L-0	T-0	P-2	C-2

***Prerequisite*:** Knowledge in DSP at PG level.

Objective: To have a thorough understanding of DSP through experimentations.

Tools :GNU Octave or MATLAB or any other equivalent tool

DSP Kits – TMS320C6X or AD or equivalent

Experiments :

Basic Processing – Transforms, Convolution and Correlation.

Random Processes – Generation of discrete time i.i.d. random processes with different distributions (Bernoulli, Binomial, Geometric, Poisson, Uniform, Gaussian, Exponential, Laplacian, Rayleigh, Rician) - pmf/pdf estimation, AR, MA and ARMA processes - spectral estimation. Visualization of Central Limit Theorem, Whitening Filter.

Numerical Computing Environments – Weiner Filtering, LMS filters, System Identification, Adaptive Equalization, Deconvolution

Multirate Signal Processing – Decimation and Interpolation, Filter bank design.

SPE 108 (P) SEMINAR

2 hours per week	L-0	T-0	P-2	C-2

***Prerequisite*:** The habit of reading technical magazines, conference proceedings and journals

Objective: To develop the skill of technical presentation and documentation.

The student shall prepare a Paper and present a Seminar on any current topic related to the branch of specialization under the guidance of a staff member. The student will undertake a detailed study based on current published papers, journals, books on the chosen subject and submit seminar report at the end of the semester. The student shall submit typed copy of the paper to the Department. Grades will be awarded on the basis of contents of the paper and the presentation. A common format in (.pdf format) shall be given for reports of Seminar and Project. All reports of Seminar and Project submitted by students shall be in this given format.

Sessional work assessment

Presentation : 25
Report : 25
Total marks : 50

SPE 201/CSP 201 DIGITAL IMAGE PROCESSING

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Knowledge in DSP and Linear Algebra at PG level.

Objective: To extend the knowledge on DSP to 2-D signal processing and hence to analyse digital images.

Image representation - Gray scale and colour Images, Representation of 2D signals, image sampling, quantization and reconstruction

Two dimensional orthogonal transforms -Digital images, Human visual perception, transforms: DFT, FFT, WHT, Haar transform, KLT, DCT.

Image enhancement - filters in spatial and frequency domains, histogram-based processing, homomorphic filtering.

Edge detection - non parametric and model based approaches, LOG filters, localization problem.

Image Restoration - PSF, circulant and block - circulant matrices, deconvolution, restoration using inverse filtering, Wiener filtering and maximum entropy-based methods.

Mathematical morphology - binary morphology, dilation, erosion, opening and closing, duality relations, gray scale morphology, applications such as hit-and-miss transform, thinning and shape decomposition.

Image and Video Compression Standards: Lossy and lossless compression schemes: Transform Based, Sub-band Decomposition, Entropy Encoding, JPEG, JPEG2000, MPEG

Computer tomography - parallel beam projection, Radon transform, and its inverse, Back-projection operator, Fourier-slice theorem, CBP and FBP methods, ART, Fan beam projection.

Image texture analysis - co-occurrence matrix, measures of textures, statistical models for textures. Hough Transform, boundary detection, chain coding, segmentation and thresholding methods.

References:

1. A. K. Jain, *Fundamentals of digital image processing,* PHI, 1989.
2. Gonzalez and Woods, *Digital image processing* ,3/E Prentice Hall, 2008.
3. R.M. Haralick, and L.G. Shapiro, *Computer and Robot Vision,* Addison Wesley, 1992.
4. R. Jain, R. Kasturi and B.G. Schunck, *Machine Vision,* MGH International Edition, 1995.

Reading:

5. W. K. Pratt, *Digital image processing,* Prentice Hall, 1989.
6. David Forsyth & Jean Ponce, *Computer Vision: A modern approach*, Pearson Edn., 2003
7. C . M. Bishop, *Pattern Recognition & Machine Learning*, Springer 2006

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 202 WAVELET THEORY

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Knowledge in DSP and Linear Algebra at PG level.

Objective: To understand the role of wavelets in signal processing.

Fourier and Sampling Theory: Generalized Fourier theory, Fourier transform, Short-time Fourier transform, Time-frequency analysis, Fundamental notions of the theory of sampling.

Theory of Frames: Bases, Resolution of unity, Definition of frames, Geometrical considerations and the general notion of a frame, Frame projector, Example – windowed Fourier frames.

Wavelets: The basic functions, Specifications, Admissibility conditions, Continuous wavelet transform (CWT), Discrete wavelet transform (DWT).

The multiresolution analysis (MRA) of $L^2(R)$: The MRA axioms, Construction of an MRA from scaling functions - The dilation equation and the wavelet equation, Compactly supported orthonormal wavelet bases - Necessary and sufficient conditions for orthonormality.

Regularity and selection of wavelets: Smoothness and approximation order - Analysis in Soboleve space, Criteria for wavelet selection with examples.

Construction of wavelets (1): Splines, Cardinal B-spline MRA, Subband filtering schemes, Compactly supported orthonormal wavelet bases.

Wavelet transform: Wavelet decomposition and reconstruction of functions in $L^2(R)$. Fast wavelet transform algorithms - Relation to filter banks, Wavelet packets – Representation of functions, Selection of basis.

Construction of wavelets (2): Biorthogonality and biorthogonal basis, Biorthogonal system of wavelets - construction, The Lifting scheme.

References:

1. Stephen G. Mallat, “A wavelet tour of signal processing” 2nd Edition Academic Press, 2000.
2. M. Vetterli, J. Kovacevic, “Wavelets and subband coding” Prentice Hall Inc, 1995
3 Gilbert Strang and Truong Q. Nguyen, “Wavelets and filter banks” Cambridge Press, 1998.
4 Gerald Kaiser, “A friendly guide to wavelets” Birkhauser/Springer 1994, Indian reprint 2005.
5 Prasad and S. Iyengar, “Wavelet analysis with applications to image processing” CRC Press, 1997.
6 J. C. Goswami and A. K. Chan, “Fundamentals of wavelets: Theory, Algorithms and Applications” Wiley-Interscience Publication, John Wiley & Sons Inc., 1999.
7 Mark A. Pinsky, “Introduction to Fourier Analysis and Wavelets” Brooks/Cole Series, 2002 .
8. R. M. Rao and A. Bopardikar, “Wavelet transforms: Introduction to theory and applications” Addison-Wesley, 1998.
9. H. L. Resnikoff and R. O. Wells, Jr., “Wavelet analysis: The scalable structure of information” Springer, 1998.
10. P. P. Vaidyanathan, “Multirate systems and filter banks” Prentice Hall P T R, 1993.
11. Michael W. Frazier, “An introduction to wavelets through linear algebra” Springer-Verlag, 1999.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 203 EMBEDDED SYSTEMS

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in Digital Electronics and Microprocessors at UG level

Objective: To develop skills in designing complex embedded systems with the help of hardware and software

Introduction to embedded hardware and software- Terminology – Gates – Timing diagram – Memory – Microprocessor buses – Direct memory access – Interrupts – Built interrupts – Interrupts basis – Shared data problems – Interrupt latency - Embedded system evolution trends – Interrupt routines in an RTOS environment.

System modeling with hardware/software partitioning- Embedded systems, Hardware/Software Co-Design, Co-Design for System Specification and modeling- Single-processor Architectures & Multi-Processor Architectures, comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification, Hardware/Software Partitioning Problem, Hardware/Software Cost Estimation, Generation of Partitioning by Graphical modeling, Formulation of the HW/SW scheduling, Optimization. Hardware/software co-synthesis- The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

Memory and interfacing: Memory write ability and storage performance – Memory types – composing memory – Advance RAM interfacing communication basic – Microprocessor interfacing I/O addressing – Interrupts – Direct memory access – Arbitration multilevel bus architecture – Serial protocol – Parallel protocols – Wireless protocols – Digital camera example.
Modes of operation – Finite state machines – Models – HCFSL and state charts language – state machine models – Concurrent process model – Concurrent process – Communication among process –Synchronization among process – Implementation – Data Flow model. Design technology – Automation synthesis – Hardware software co-simulation – IP cores – Design Process Model.

References:

1. David. E. Simon, “An Embedded Software Primer”, Pearson Education, 2001.

2. Tammy Noergaard, “Embedded System Architecture, A comprehensive Guide for Engineers and Programmers”, Elsevier, 2006.

3. Raj Kamal, “Embedded Systems- Architecture, Programming and Design”, Tata McGraw Hill, 2006.

4. Frank Vahid and Tony Givargis „Embedded Systems Design: A Unified Hardware/Software Introduction, John & Wiley Publications, 2002.

5. Steve Heath, “Embedded System Design”, Elsevier, Second Edition, 2004.

6. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.

7. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Pub, 1997.

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SPE 204 (A)/CSP 204 (A) STATISTICAL SIGNAL PROCESSING

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in probability, matrices and DSP at UG level.

Objective: To have a good foundation in statistical signal processing.

Review of fundamentals: Correlation matrix - properties - physical significance. Eigen analysis of matrix, structure of matrix and relation with its eigen values & eigen vectors. Spectral decomposition of corr. matrix, positive definite matrices - properties - physical significance. Complex Gaussian processes, MA, AR, ARMA processes and their properties, method of Lagrange multipliers.

LMMSE Filters: Goal of adaptive signal processing, some application scenarios, problem formulation, MMSE predictors, LMMSE predictor, orthogonality theorem (concept of innovation processes), Yule-walker equation, Wiener Solution, Iterative solution of Wiener-Hopf's equation, Levinson Durbin Algorithm (LDA), inverse LDA, Method of steepest descent and its convergence criteria. Kalman Filter (KF), recursions, Extended KF, comparison of KF and Weiner filter.

Adaptive filters: Filters with recursions - the steepest descent - Newton's method, criteria for the convergence, rate of convergence. LMS filter, mean and variance of LMS, the MSE of LMS and misadjusment, Criteria for convergence and LMS versions: normalized LMS, leaky, sign, variable stepsize, filtered input LMS and complex LMS algorithms. Transform domain LMS algorithm using DFT and DCT, its performance improvement over LMS and Newton's LMS algorithm .

Subband LMS adaptive filters: multirate concepts, decimation, interpolation, perfect reconstruction, oversampled filter bank design and delayless subband adaptive filter. Block LMS algorithm(BLMS): Frequency domain BLMS(FBLMS), constrained FBLMS, partitioned FBLMS, delayless FBLMS, iterated FBLMS.

IIR adaptive filters- output error method, equation error method, their problems and solutions. Recursive Least Square (RLS) method, fast transversal, fast lattice RLS and affine projection algorithms. Tracking performance of the time varying filters: Tracking performance of LMS and RLS filters. Applications : Spectral Estimation, System identification, channel equalization, noise and echo cancellation.

References:

1. B. Farhang-Boroujeny, Adaptive filters: Theory and Applications, John-Wiley, 1998
2. S. Haykin. (1986). *Adaptive Filters Theory*. Prentice-Hall.
3. Dimitris G. Manolakis, Vinay K. Ingle, Stephan M Krgon, *Statistical and Adaptive Signal Processing*, McGraw Hill (2000)

Reading:

4. Jones D. *Adaptive Filters* [Connexions Web site]. May 12, 2005. Available at: http://cnx.rice.edu/content/col10280/1.1/

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 204 (B) CMOS MIXED SIGNAL CIRCUIT DESIGN

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in MOSFETs and Analog Integrated Circuit Design.

Objective: To have in depth knowledge in the analysis and design of mixed signal circuits.

PLL and switched capacitor circuits-Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL - simple PLL, charge-pump PLL, applications of PLL-Switched Capacitor circuits - basic principles, some practical circuits such as switched capacitor integrator, biquad circuit, switched capacitor filter, switched capacitor amplifier, non-filtering applications of switched capacitor circuit such as programmable gate arrays, DAC and ADC, MOS comparators, modulators, rectifiers, detectors, oscillators.

Sampling circuits: Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures: Open-loop & closed-loop architectures, open-loop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture.

ADC&DAC-Input/output characteristics and quantization error of an A/D converter, performance metrics of A/D converter. A/D converter architectures: Flash architectures, two-step architectures, interpolate and folding architectures, pipelined architectures, Successive approximation architectures, interleaved architectures. Input/output characteristics of an ideal D/A converter, performance metrics of D/A converter, D/A converter in terms of voltage, current, and charge division or multiplication, switching functions to generate an analog output corresponding to a digital input. D/A converter architectures: Resistor-Ladder architectures, current-steering architectures.

Filters-Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-C integrator, discrete time integrators. Filtering topologies - bilinear transfer function and biquadratic transfer function.

References:

1. Razavi, "Design of analog CMOS integrated circuits", McGraw Hill, 2001.
2. Razavi, "Principles of data conversion system design", S. Chand and company ltd, 2000.
3. Jacob Baker, "CMOS Mixed-Signal circuit design", IEEE Press, 2002.
4. Gregorian, Temes, "Analog MOS Integrated Circuit for signal processing", John Wiley & Sons 5. Baker, Li, Boyce, "CMOS : Circuit Design, layout and Simulation", PHI, 2000.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 204 (C) MULTIMEDIA SYSTEMS

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Knowledge in digital image processing and speech processing at PG level.

Objective: To have an indepth knowledge of Multimedia Systems.

Multimedia Data Representations: Basics of Digital Audio - Digitization of Sound, Typical Audio Formats (.au, .wav) Introduction to MIDI.

Graphic/Image File Formats - Graphic/Image Data Structures. Standard System Independent Formats (GIF, JPEG, TIFF, PNG, PS, EPS).System Dependent Formats (XBM, BMP).

Color in Image and Video - Basics of Color. Human visual system, Rods and Cones. Color Models in Images (RGB, CMY). Color Models in Video (RGB, YUV, YCrCb).

Basics of Video - Types of Color Video Signals, Analog Video, Digital Video.

Basics of Signal Compression: Lossless Compression Algorithms - Basics of Information Theory. Huffman Coding. Adaptive Huffman Coding. Lempel-Ziv-Welch Algorithm.

Lossy Image Compression – Overview of JPEG. JPEG 2000

Audio Compression: Simple Audio Compression Methods. Psychoacoustics. Overview of Audio Standards - MPEG, AAC, AC3.

Video Compression: Fundamentals of Lossy Video Compression - Intra Frame and Inter Frame redundancy. Motion estimation techniques. Motion compensation. Intra Frame Prediction. Faster algorithms for motion estimation. De-blocking. Rate Control. Overview of Video Standards – MPEG video standards, Video Teleconferencing Standards.

References:

1. V. Bhaskaran and K. Konstantinides, "Image and Video Compression Standards: Algorithms and Architectures", 2nd ed., *Kluwer Academic Publishers*, 1997.
2. Steinmetz, Ralf; Nahrstedt, Klara, "Multimedia Fundamentals, Volume 1: Media Coding And Content Processing", Pearson Education India, 2002
3. Keith Jack, "Video Demystified: A Handbook for the Digital Engineer", 4th ed, Newnes, 2004.
4. Symes, Peter D, "Video Compression Demystified", McGraw-Hill, 2001
5. K.R. Rao, Zoran S. Bojkovic, Dragorad A Milovanovic – *Multimedia Communication Systems: Techniques, Standards and Networks*- Prentice Hall.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 204 (D) ASIC DESIGN

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in Digital System Design at UG level

Objective: To develop the skills in designing using application specific ICs.

Introduction to ASICs- CMOS logic ans ASIC library .Types of ASICs - Design flow - CMOS transistors, CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

Programmable ASICs- logic cells and I/O cells. Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX. DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks. Programmable ASIC interconnects– Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

Logic synthesis, simulation and testing-Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation, Introduction to JTAG.

ASIC construction- Floor planning, placement and Routing. System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

References:

1. M.J.S .Smith, "Application Specific Integrated Circuits ", Addison -Wesley Longman Inc., 1997.
2. Andrew Brown, "VLSI Circuits and Systems in Silicon", McGraw Hill, 1991
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Vranesic, “Field Programmable Gate Arrays”, Kluwer Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", McGraw Hill, 1994.
5. S. Y. Kung, H. J. White House, T. Kailath, "VLSI and Modern Signal Processing ", Prentice Hall, 1985.
6. Jose E. France, YannisTsividis, "Design of Analog & Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 205 (A) SPEECH PROCESSING

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Knowledge in DSP at PG level.

Objective: To form a good platform in various processing methodologies of speech signal.

Digital models for the speech signal - mechanism of speech production - acoustic theory - lossless tube models - digital models - linear prediction of speech - auto correlation - formulation of LPC equation - solution of LPC equations - Levinson Durbin algorithm - Levinson recursion - Schur algorithm - lattice formulations and solutions - PARCOR coefficients - Spectral analysis of speech - Short Time Fourier analysis - filter bank design. Auditory Perception : Psychoacoustics- Frequency Analysis and Critical Bands - Masking properties of human ear.

Speech coding -subband coding of speech - transform coding - channel vocoder - formant vocoder - cepstralvocoder - vector quantizer coder- Linear predictive Coder. Speech synthesis - pitch extraction algorithms - gold rabiner pitch trackers - autocorrelation pitch trackers - voice/unvoiced detection - homomorphic speech processing - homomorphic systems for convolution - complex cepstrums - pitch extraction using homomorphic speech processing. Sound Mixtures and Separation - CASA, ICA & Model based separation.

Speech Transformations - Time Scale Modification - Voice Morphing. Automatic speech recognition systems - isolated word recognition - connected word recognition -large vocabulary word recognition systems - pattern classification - DTW, HMM - speaker recognition systems - speaker verification systems - speaker identification Systems.

Audio Processing : Non speech and Music Signals - Modeling -Differential, transform and subband coding of audio signals & standards - High Quality Audio coding using Psychoacoustic models - MPEG Audio coding standard. Music Production - sequence of steps in a bowed string instrument - Frequency response measurement of the bridge of a violin. Audio Data bases and applications - Content based retrieval.

References:

1. Rabiner L.R. & Schafer R.W., “Digital Processing of Speech Signals”, Prentice Hall Inc.

2. O'Shaughnessy, D. “Speech Communication, Human and Machine”. Addison-Wesley.

3. Thomas F. Quatieri , “Discrete-time Speech Signal Processing: Principles and Practice” PH.

4. Deller, J., J. Proakis, and J. Hansen. “Discrete-Time Processing of Speech Signals.” Macmillan.

5. Ben Gold & Nelson Morgan , “ Speech and Audio Signal Processing”, John Wiley & Sons, Inc.

6. Saito S. & Nakata K., “Fundamentals of Speech Signal Processing”, Academic Press, Inc.

7. Papamichalis P.E., “Practical Approaches to Speech Coding”, Texas Instruments, Prentice Hall

8. Jayant, N. S. and P. Noll. “Digital Coding of Waveforms: Principles and Applications to Speech and Video. Signal Processing Series”, Englewood Cliffs: Prentice-Hall.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 205 (B) LOW POWER VLSI DESIGN

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in Digital VLSI Design.

Objective: To develop the skills in designing circuits with low power consumption.

Review of power dissipation in CMOS Circuits – static and dynamic power dissipation-Leakage sources, input vector dependence, stack effect, leakage reduction using natural and forced stacks, power gating, power gating methodologies, dynamic voltage scaling, forward and reverse body bias, standby techniques, MTCMOS circuits, level shifters, timing and power planning, choosing the high V_{TH} value, MTCMOS circuits using sleep transistors.

Supply voltage scaling approaches: parallelism, pipelining, using multiple supply voltage, module level voltage selection, clustered voltage scaling, level converters, multiple supplies inside a block, supply voltage limitations, Optimum supply voltage, multiple device threshold, Technology level – feature size scaling, threshold voltage scaling, Transistor sizing for energy minimization, dynamic supply voltage scaling, dynamic threshold voltage scaling.

Switching activity estimation in static and dynamic logic: signal statistics, inter signal correlations, Reducing switching capacitance through transistor sizing, logic and architecture optimization, layout techniques, logic restructuring, input ordering, data representation, resource allocation, reducing glitching through path balancing, clock gating.

Behavioral level transforms, algorithm level transforms, architectural transformations, Operation reduction and substitution, logic level optimization and technology mapping, Energy recovery, design with reversible logic, adiabatic logic, peripheral circuits, Power gating, signal isolation, state retention and restoration, architectural issues for power gating, Dynamic voltage and frequency scaling.

References:

1. Anantha Chandrakasan, Robert Brodersen, Low-power CMOS design, IEEE press, 1998
2. Kaushik Roy, Sharat C. Prasad, Low-power CMOS VLSI circuit design, John Wiley & Sons, 2000.
3.A.Bellamour, M.I.Elmasri, Low power VLSI CMOS circuit design, Kluwer Academic Press, 1995
4. Siva G.Narendran, Anantha Chandrakasan, Leakage in Nanometer CMOS Technologies, Springer, 2005.
5. Mohab Anis, Mohamed Elmasry, Multi-Threshold CMOS Digital Circuits, Kluwer Academic Publishers, 2003.
6. Michael Keating, David Flynn, Robert Aitken, Alan Gibbons and Kaijian Shi, Low power methodology manual, Springer, 2008.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 205 (C) BIOMETRIC PROCESSING

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Knowledge in digital signal processing and digital image processing at PG level.

Objective: To investigate the scope of biometrics in technology.

Introduction: Biometrics – features – usefulness in security systems
Fingerprints: Analysis and Representation, Matching, Classification and Indexing, Non-linear deformation, mosaicing, One recent paper on Fingerprints
Iris: Analysis using texture-based methods
Face: Detection, tracking and recognition. One recent paper on Face Detection
Speech Recognition. One recent paper on Speech Recognition
Multimodal Biometrics: Fusion techniques, score normalization. Security: Biometric watermarking. One recent paper on Biometric based Security Systems.

References:

1. Handbook of Fingerprint Verification, D Maltoni, D Maio, AK Jain, S Prabhakar, Springer Verlag, 2003
2. Biometric Authentication: A Machine Learning Approach, S.Â Y.Â Kung, M.Â W.Â Mak, S.Â H.Â Lin, Prentice Hall PTR, 2004
3. Introduction to Biometrics and Network Security, Paul Reid, Prentice Hall PTR, 2004
4. Computer Vision, A Modern Approach, David A. Forsyth, Jean Ponc, Prentice Hall, 2002

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SPE 205 (D) INTRODUCTION TO NANO ELECTRONICS

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in Solid State Devices at UG level

Objective: To have in depth knowledge in usage and working of nano-meter scale devices.

Challenges going to sub-100 nm MOSFETs – Oxide layer thickness, tunneling, power density, non-uniform dopant concentration, threshold voltage scaling, lithography, hot electron effects, sub-threshold current, velocity saturation, interconnect issues, fundamental limits for MOS operation. High-K gate dielectrics, effects of high-K gate dielectrics on MOSFET performance,

Novel MOS-based devices – Multiple gate MOSFETs, Silicon-on-nothing, Silicon-on-insulator devices, FD SOI, PD SOI, FinFETs, vertical MOSFETs, strained Si devices

Hetero structure based devices – Type I, II and III Heterojunction, Si-Geheterostructure, hetero structures of III-V and II-VI compounds - resonant tunneling devices, MODFET/HEMT

Carbon nanotubes based devices – CNFET, characteristics, Spin-based devices – spin FET, characteristics

Quantum structures – quantum wells, quantum wires and quantum dots, Single electron devices – charge quantization, energy quantization, Coulomb blockade, Coulomb staircase, Bloch oscillations

References:

1. Mircea Dragoman and Daniela Dragoman, Nanoelectronics – Principles & devices, Artech House Publishers, 2005.
2. Karl Goser, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer 2005.
3. Mark Lundstrom and Jing Guo, Nanoscale Transistors: Device Physics, Modeling and Simulation, Springer, 2005.
4. Vladimir V Mitin, Viatcheslav A Kochelap and Michael A Stroscio, Quantum heterostructures, Cambridge University Press, 1999.
5. S.M. Sze (Ed), High speed semiconductor devices, Wiley, 1990.
6. ManijehRazeghi, Technology of Quantum Devices, Springer, ISBN 978-1-4419-1055-4.
7. H.R. Huff and D.C. Gilmer, High Dielectric Constant Materials for VLSI MOSFET Applications, Springer 2005, ISBN 978-3-540-21081-8 , (Available on NITC intranet in Springer eBook section)
8.B.R. Nag, Physics of Quantum Well Devices, Springer 2002, ISBN 978-0-7923-6576-1, (Available on NITC intranet in Springer eBook section).
9. E.Kasper, D.J. Paul, Silicon Quantum Integrated Circuits Silicon-Germanium Heterostructures Devices: Basics and Realisations, Springer 2005, ISBN 978-3-540-22050-3,

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 206 (A) PATTERN RECOGNITION AND COMPUTER VISION

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Knowledge in probability, linear algebra and DSP at PG level.

Objective: To achieve a thorough knowledge in pattern recognition and machine vision.

Introduction - features, feature vectors and classifiers, Supervised versus unsupervised pattern recognition. Classifiers based on Bayes Decision theory- introduction, discriminant functions and decision surfaces, Bayesian classification for normal distributions, Estimation of unknown probability density functions, the nearest neighbour rule. Linear classifiers,- Linear discriminant functions and decision hyper planes, The perceptron algorithm, MSE estimation, Logistic determination, Support Vector machines.

Non-Linear classifiers - Two layer and three layer perceptrons, Back propagation algorithm, Networks with Weight sharing, Polynomial classifiers, Radial Basis function networks, Support Vector machines-nonlinear case, Decision trees, combining classifiers, Feature selection, Receiver Operating Characteristics (ROC) curve, Class separability measures, Optimal feature generation, The Bayesian information criterion.

Feature Generation (1) - Linear transforms-KLT, SVD, ICA, DFT, DCT, DST, Hadamard Transform, Wavelet Transform, Wavelet Packets - Two dimensional generalizations - Applications.

Feature Generation (2) - regional features, features for shape and characterization, Fractals, typical features for speech and audio classification, Template Matching, Context dependent classification- Bayes classification, Markov chain models, HMM, Viterbi Algorithm. System evaluation - Error counting approach, Exploiting the finite size of the data.

Clustering - Cluster analysis, Proximity measures, Clustering Algorithms - Sequential algorithms, Neural Network implementation. Hierarchical algorithms - Agglomerative algorithms, Divisive algorithms. Schemes based on function optimization - Fuzzy clustering algorithms, Probabilistic clustering, K - means algorithm. Clustering algorithms based on graph theory , Competitive learning algorithms, Binary Morphology Clustering Algorithms Boundary detection methods, Valley seeking clustering, Kernel clustering methods. Clustering validity.

References:

1. Sergios Theodoridis, Konstantinos Koutroumbas, “Pattern Recognition”, Academic Press, 2006.
2. Duda and Hart P.E, Pattern classification and scene analysis, John Wiley and sons, NY, 1973.
3. E. Gose, R. Johnsonbaugh, and S. Jost, Pattern Recognition and Image Analysis, PHI, 1999.
4. Fu K.S., Syntactic Pattern recognition and applications, Prentice Hall, Eaglewood cliffs, N.J., 1982
5. R. O. Duda, P. E. Hart and D. G. Stork, Pattern classification, John Wiley & Sons Inc., 2001
6. Andrew R. Webb, “ Statistical Pattern Recognition”, John Wiley & Sons, 2002

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 206 (B)/CSP 206 (C) RESEARCH METHODOLOGIES

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in research/project work at UG level

Objective: To gain knowledge in making research proposals and writing technical papers.

Introduction – Meaning of research – Objectives of research – Motivation in research – Types of research – Research approaches – Significance of research – Research methods vs Methodology – Criteria of good research.

Defining Research Problem – What is a research problem – Selecting the problem – Necessity of defining the problem – Literature review – Importance of literature review in defining a problem – Critical literature review – Identifying gap areas from literature review

Research design – Meaning of research design – Need– Features of good design – Important concepts relating to research design – Different types – Developing a research plan

Method of data collection – Collection of data- observation method – Interview method – Questionnaire method – Processing and analysis of data – Processing options – Types of analysis – Interpretation of results

Report writing – Types of report – Research Report, Research proposal ,Technical paper – Significance – Different steps in the preparation – Layout, structure and Language of typical reports – Simple exercises – Oral presentation – Planning – Preparation – Practice – Making presentation – Answering questions - Use of visual aids – Quality & Proper usage – Importance of effective communication – Illustration

References:

1. Coley S M and Scheinberg C A, 1990, *"Proposal Writing",* Newbury Sage Publications.
2. Leedy P D, *"Practical Research : Planning and Design",* 4th Edition, N W MacMillan Publishing Co.
3. Day R A, *"How to Write and Publish a Scientific Paper",* Cambridge UniversityPress,1989.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 206 (C) EMBEDDED NETWORKS

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in Microprocessors/Microcontrollers and Communication Networks at UG level

Objective: To attain good skills in designing embedded system networks.

Embedded communication protocols. Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

USB and CAN bus.USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN

Ethernet-Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

Wireless embedded networking- Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

References:

1. Frank Vahid, Tony Givargis Embedded Systems Design: A Unified Hardware/Software Introduction, John & Wiley Publications,2002

2. Jan Axelson, Parallel Port Complete: Programming, interfacing and using the PC‟s parallel printer port , Penram publications, 1996.

3. Dogan Ibrahim, Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series, Elsevier 2008.

4. Jan Axelson Embedded Ethernet and Internet Complete, Penram publications, 2003.

5. Bhaskar Krishnamachari, Networking Wireless Sensors, Cambridge press 2005.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 206 (D) VLSI SYSTEM DESIGN

3 hours lecture per week	L-3	T-0	P-0	C-3

***Prerequisite*:** Basic knowledge in Digital System Design at UG level

Objective: To have a good understanding in application specific integrated circuit design

Introduction to digital IC design – Custom and semicustom flow, combinational logic synthesis – Technology independent and technology dependent optimization –Logic synthesis -High level synthesis- Scheduling and allocation-ASAP and ALAP scheduling-Register allocation-Functional unit allocation-Interconnect path allocation-Hardware description languages-synthesis-register transfer design-Event driven simulation.

Subsystem design principles - pipelining-Data paths in processor architecture – Standard cell layout-Logic design considerations of adder and multiplier- Timing -Slack delay model – Effect of skew and jitter on timing, Sources of skew and jitter- Clocking disciplines -Wire model- Technology scaling effect on interconnect and -Noise in interconnects.

Partitioning and routing - Floorplanning and pin assignment-Slicing tree –Channel definition-Channel routing order-Wind mill constraint-Placement-Special routing-Clock routing for regular and irregular structures-Power routing-Global routing-Line Probe algorithm-Maze routing-Detail routing-Left edge algorithm-Vertical constraint-switch box routing.

FPGA logic element and interconnect architecture - logic synthesis for FPGA-Physical design for FPGA-I/O circuits, ESD protection, Off chip connections.

References:

1. James R.Armstrong, F.Gail Gray, VHDL Design Representation and Synthesis, Pearson education, 2007.
2. M.J.S .Smith, "Application Specific Integrated Circuits ", Addison -Wesley Longman Inc., 1997.
3. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Prentice Hall, Second Edition, 2005.
4. Wayne Wolf, FPGA-Based System Design, Pearson, 2009.
5. Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation, Springer, Third edition,1999.

Question Pattern: There would be 7 questions out of which 5 should be answered. Each question would carry 20 marks each. Each question shall carry a maximum of four sub sections which can have uneven distribution of marks. The questions would touch upon all the sections of the syllabus as far as possible and would preferably be analytic in nature.

SPE 207 (P) VLSI & EMBEDDED SYSTEMS LAB

2 hours practical per week	L-0	T-0	P-2	C-2

***Prerequisite*:** Basic knowledge in Digital System Design and Design with Embedded processors.

Objective: To attain practical skills in digital/analog system design

FPGA based Experiments:

1. Design Entry Using Verilog/VHDL examples for circuit description. Sequential and concurrent statements.

2. Structural and behavioral descriptions, principles of operation and limitation of HDL simulators. Examples of sequential and combinational logic design and simulation. Test vector generation.

3. Synthesis principles, logical effort, standard cell based design and synthesis, interpretation synthesis scripts, constraint introduction and library preparation and generation.

4. FPGA programming, I/O interfacing, Analog interfacing, Real time application development.

Microcontroller based Experiments:

1. Design with Microcontrollers- PIC Microcontrollers- Assembly and C Programming: I/O Programming, Timers.

2. Interrupts, Serial port programming.

3. PWM Generation, Motor Control, ADC/DAC.

4. LCD and RTC Interfacing, Sensor Interfacing.

5. Design with ARM Processors: I/O programming, ADC/DAC, Timers, Interrupts

6. Study of one type of Real Time Operating Systems (RTOS)

SPE 208 (P) TERM PAPER

2 hours per week	L-0	T-0	P-2	C-2

***Prerequisite*:** The habit of reading technical magazines, conference proceedings and journals

Objective: To develop the skill of technical presentation and documentation and motivation for doing research work.

The student is expected to present a report on the literature survey conducted as a prior requirement for the project to be taken up in the third and fourth semesters. Head of department can combine TP hours of many weeks and allot a maximum of 4 weeks exclusively for it. Students should execute the project work using the facilities of the institute. However, external projects can be taken up, if that work solves a technical problem of the external firm. Prior sanction should be obtained from the head of department before taking up external project work. Project evaluation committee should study the feasibility of each project work before giving consent. An overview on the project work should be introduced before the closure of first semester. A paper should be prepared based on the project results and is to publish in refereed Conferences/Journals. Grades will be awarded on the basis of contents of the paper and the presentation.

Sessional work assessment
Presentation: 25
Report: 25
Total marks : 50

SPE 301 THESIS – PRELIMINARY

22 hours per week	L-0	T-0	P-22	C-8

This shall comprise of two seminars and submission of an interim thesis report. This report shall be evaluated by the evaluation committee. The fourth semester Thesis-Final shall be an extension of this work in the same area. The first seminar would highlight the topic, objectives, methodology and expected results. The first seminar shall be conducted in the first half of this semester. The second seminar is presentation of the interim thesis report of the work completed and scope of the work which is to be accomplished in the fourth semester.

Weightages for the 8 credits allotted for the Thesis-Preliminary

Evaluation of the Thesis-Preliminary work: by the guide - 50% (200 Marks)

Evaluation of the Thesis–Preliminary work: by the Evaluation Committee-50%(200 Marks)

SPE 401 THESIS

22 hours per week	L-0	T-0	P-22	C-12

Towards the end of the semester there shall be a pre submission seminar to assess the quality and quantum of the work by the evaluation committee. This shall consist of a brief presentation of Third semester interim thesis report and the work done during the fourth semester. At least one technical paper is to be prepared for possible publication in journals / conferences. The final evaluation of the thesis shall be an external evaluation. The 12 credits allotted for the Thesis-Final may be proportionally distributed between external and internal evaluation as follows.

Weightages for the 12 credits allotted for the Thesis

Internal Evaluation of the Thesis work: by the guide - (200 Marks)
Internal Evaluation of the Thesis work: by the Evaluation Committee - (200 Marks)

Final Evaluation of the Thesis work by the Internal and External Examiners:-
(Evaluation of Thesis + Viva Voce) - (100+100 Marks)